IN THE SPECIFICATION

Please replace the paragraph and subparagraphs beginning at page 6, line 10, through page 7, line 2, with the following rewritten paragraph:

~~A semiconductor memory device according to an aspect of the present invention comprises:~~

~~word lines formed along a first direction;~~

~~bit lines formed along a second direction which intersects the first direction;~~

~~memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines;~~

~~a row decoder which selects at least one of the word lines;~~

~~a column decoder which selects at least one of the bit lines; and~~

~~a write circuit which supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder respectively and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line, the write circuit changing the current values of the first and second write currents according to a temperature change.~~

A semiconductor memory device according to an aspect of the present invention includes: word lines formed along a first direction; bit lines formed along a second direction which intersects the first direction; memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines; a row decoder which selects at least one of the word lines; a column decoder which selects at least one of the bit lines; and a write circuit which supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder respectively and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line, the write circuit including first and second current sources whose supply

currents have different temperature dependencies, the first and second current sources being set to be one of an enable state and a disable state in accordance with an ambient temperature, at least one of current values of the first and second write currents being controlled in accordance with the supply currents of the first and second current sources.

Please replace the paragraph and subparagraphs beginning at page 7, line 24, through page 8, line 18, with the following rewritten paragraph:

~~A memory card according to an aspect of the present invention comprises at least one semiconductor memory cell block,~~

~~the semiconductor memory cell block including:~~

~~word lines formed along a first direction;~~

~~bit lines formed along a second direction which intersects the first direction;~~

~~memory cells including magneto-resistive elements and arranged at intersections of the word lines and the bit lines;~~

~~a row decoder which selects at least one of the word lines;~~

~~a column decoder which selects at least one of the bit lines; and~~

~~a write circuit which supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder respectively and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line, the write circuit changing the current values of the first and second write currents according to a temperature change.~~

A memory card according to an aspect of the present invention includes at least one semiconductor memory cell block, the semiconductor memory cell block including: word lines formed along a first direction; bit lines formed along a second direction which intersects the first direction; memory cells including magneto-resistive elements and arranged at

intersections of the word lines and the bit lines; a row decoder which selects at least one of the word lines; a column decoder which selects at least one of the bit lines; and a write circuit which supplies first and second write currents to a selected word line and selected bit line selected by the row decoder and column decoder respectively and writes data into a selected memory cell arranged at the intersection of the selected word line and the selected bit line, the write circuit including first and second current sources whose supply currents have different temperature dependencies, the first and second current sources being set to be one of an enable state and a disable state in accordance with an ambient temperature, at least one of current values of the first and second write currents being controlled in accordance with supply currents of the first and second current sources.

Please amend the paragraph beginning at page 105, line 22, to page 107, line 14, as follows:

First, the pass bit number storing register 640 is initialized ~~(step S10)~~ and the write current setting register 660 is initialized (step S11). As described before, in order to detect the optimum write current, whether the write operation is successfully performed or not is checked while the write current is being changed. Therefore, it is necessary to perform the checking process by use of a plurality of write currents. However, the number of combinations of the write currents I1, I2 is limitless. Therefore, for example, a plurality of ratios I1/I2 are selected and several observation points are set for each ratio I1/I2. Specifically, the combinations of the write currents I1, I2 are selected as shown in FIG. 52. FIG. 52 is a graph showing the combinations of the write currents I1, I2. As shown in FIG. 52, the write currents I1, I2 which satisfy the relations of I1/I2 = c1, c2, c3, c4 are selected. Then, 27 combinations of (I1, I2) which satisfy the relations of I1/I2 are selected on four lines extending from the origin (I1 = I2 = 0). That is, the write operation into the memory cell is

performed by use of the 27 combinations of (I1, I2). The combinations are referred to as observation points P1 to P27 as shown in FIG. 52. Initialization of the write current setting register 660 means that values of (I1, I2) used at the first write operation are stored in the write current setting register 660. For example, in FIG. 52, the currents (I1, I2) in the observation point P1 are stored in the write current setting register 660. Further, initialization of the pass bit number storing register 640 indicates the following matter. In order to detect the optimum write current, a data pattern is written into the memory cell array 11 by use of the write currents (I1, I2) at the observation points stored in the write current setting register 660. Then, the number of memory cells (pass bit) into which data is correctly written in the memory cell array 11 is counted and values of (I2, I2) corresponding to the largest count number are determined as the optimum write currents. In the initialization process of the write current setting register 660 in the step S1, the present pass bit number to be compared with the pass bit number obtained when the write operation is performed at the first observation point P1 is stored in the write current setting register 660 and the pass bit number may be zero, for example.